Amendments to the Specification

At pages 9-11, please delete paragraphs **[0014]** and **[0015]** and replace them with the following paragraphs:

[0014] Figure 3 illustrates the relationship between the component clock signals 202_1-202_4 and a DDR input signal 302 after the CDR circuit 200 has achieved phase lock. As shown, a rising edge of the data clock signal 202_1 occurs at the midpoint of each even phase data eye (i.e., each even-numbered data valid interval within DDR input signal 302) and is used to enable the corresponding sampling circuit 223_1 to sample (i.e., latch or capture the state of) the even phase data value. Each successive sample captured by the sampling circuit 221_1 is shifted into the shift register 223_1 such that, in the case of a DDR input signal, the shift register 223_1 is reloaded with a new set of N even phase data samples every N cycles of the recovered clock signal 202. Similarly, rising edges of the complement data clock signal ~~221_2~~ 202_3 occur at the midpoints of odd phase data eyes in the DDR input signal 302 such that shift register 223_2 is reloaded with a new set of N odd phase data samples every N cycles of the recovered clock signal 202. Rising edges of the edge clock signal ~~202_3~~ 202_2 are aligned with even-to-odd data transitions in the DDR input signal 302 (i.e., the edge clock transitions are aligned with edges of the data eyes) such that, if an odd phase data value is different from the preceding even phase data value (a data state transition), the signal sample captured in response to the edge clock signal ~~202_3~~ 202_2 (i.e., the edge clock sample) indicates whether the edge clock signal ~~202_3~~ 202_2, and therefore all the component clock signals of the recovered clock signal, has transitioned early or late relative to the transition in the input signal 302. That is, an edge clock sample that is equal to the even phase data sample indicates that the edge clock signal transitioned nearer to the even phase data eye than the odd phase data eye and therefore that the recovered clock signal 202 is advanced relative to (i.e., leads) the transition point of the input signal 302. Conversely, an edge clock sample that is equal to the odd phase data sample indicates that the edge clock signal transitioned nearer to the odd phase data eye than the even phase data eye, and therefore that the recovered clock signal 202 lags the transition point of the input signal 302. Rising edges of the complement edge clock signal ~~203_4~~ 202_4 are aligned with odd-to-even data transitions and therefore provide corresponding lead-lag information when a data state change occurs between odd-to-even data phases of the input signal 302.

[0015] Figure 4 illustrates the phase relationship between DDR and SDR input signals (302 and 402, respectively), and edges of the component clock signals 202_1-202_4. As shown, edges in data clock signal

202_1 that are used to sample even phase data within the DDR signal 302 are centered (when the CDR circuit is phase locked to an SDR input data signal) within both even and odd phase data eyes of the SDR input signal. Also, edges in the complementary data clock signal occur at transition points between successive data eyes within the SDR signal 402. From this observation, it follows that data state information within the SDR signal 402 is captured by sampling circuit 221_1 (i.e., in response to transitions in data clock signal 202_1), while data transition information within the SDR signal is captured by sampling circuit 221_2. Thus, lead-lag information may be obtained from a SDR input signal by comparing successive data state samples captured by sampling circuit 221_1 to determine whether a state transition has occurred and, if so, checking for equality between the intervening data transition sample (captured by sampling circuit 221_2) and either the preceding or succeeding data state sample to determine whether the complementary data clock signal ~~202_2~~ 202_3 (and therefore all the components of the recovered clock signal 202) leads or lags the input signal transition. Note that in an alternative embodiment, the edge clock signal ~~202_3~~ 202_2 and complement edge clock signal 202_4 may be used to obtain data state and data transition samples, respectively, instead of clock signals 202_1 and 202_2.